AND8266/D

Designing NCP1337

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APPLICATION NOTE

Description

NCP1337 is a valley−switching controller offering various features making it ideal to build efficient quasi−resonant power supplies. It incorporates a wealth of protective features that eases the design of any specific application and the compliance to the specifications of modern power supplies, including reliability and standby efficiency.

This controller is the ideal candidate where low part−count is the key parameter, particularly in AC/DC adapters, consumer electronics or auxiliary supplies.

Features

- Quasiresonant Operation: Valley−switching operation is ensured whatever the operating conditions are, thanks to the internal Soxyless circuitry. As a result, there are virtually no primary switch turn−on losses and no secondary diode recovery losses, and EMI and video noise perturbations are reduced. The converter also stays a first−order system and accordingly eases the feedback loop design.
- Dynamic Self−Supply (DSS): Due to its Very High Voltage Integrated Circuit (VHVIC) technology, ON Semiconductor's NCP1337 allows for a direct pin connection to the high−voltage DC rail. A dynamic current source charges up a capacitor and thus provides a fully independent V_{CC} level. As a result, low power applications will not require any auxiliary winding to supply the controller. In applications where this winding is anyway required, the DSS will simplify the V_{CC} capacitor selection.
- Overcurrent Protection (OCP): When the feedback voltage is at its maximum value, a fault is detected. If this fault is present for more than 80 ms, NCP1337 enters an auto−recovery soft burst mode. All pulses are stopped and the V_{CC} capacitor discharges down to 5.0 V. Then, by monitoring the V_{CC} level, the startup current source is activated ON and OFF to create a burst mode. After the current source being activated twice, the controller tries to restart, with a 4 ms soft−start. If the fault has gone, the SMPS resumes operation. If the fault is still there, the burst sequence starts again. The soft−start together with a minimum frequency clamp allow to reduce the noise generated in the transformer in short−circuit conditions.
- Over Voltage Protection (OVP): By continuously monitoring the V_{CC} voltage level, the NCP1337 stops switching whenever an over−voltage condition is detected
- Brown−out Detection (BO): By monitoring the level on pin 1 during normal operation, the controller protects the SMPS against low mains condition. When pin 1 voltage falls below 500 mV, the controller stops pulsing until this level goes back and resumes operation. By adjusting the resistor divider connected between the high input voltage and this pin, start and stop levels are programmable.
- Overpower Compensation (OPC): An internal current source injects out of Pin 3 (CS pin) a current proportional to the voltage applied on pin 1. As this voltage is an image of the input voltage, by inserting a resistor in series with Pin 3, it is possible to create an offset on the current sense signal that will compensate the effect of the input voltage variation.
- External Latch Trip Point: By externally forcing a level on pin 1 (e.g. with a signal coming from a temperature sensor) greater than 3 V (but below 5 V), it is possible to disable the output of the controller. Once the voltage goes back below 3 V, the controller is enabled and starts. If the voltage is forced over 5 V, the controller is permanently latched−off: to resume normal operation, the V_{CC} voltage should go below 4 V, which implies to unplug the SMPS from the mains.
- Standby Ability: Under low load conditions, NCP1337 enters a soft ripple mode: when the CS setpoint becomes lower than 20% of the maximum peak current, output pulses are stopped, then switching is starting again when FB loop forces a setpoint higher than 25%. As this occurs at low peak current, with soft−skip activated, and as the T_{OFF} is clamped, noise−free operation is guaranteed, even with a cheap transformer.

TYPICAL APPLICATION

The above features makes NCP1337 well suited for offline applications of a wide power range. A typical application is shown in Figure 1.

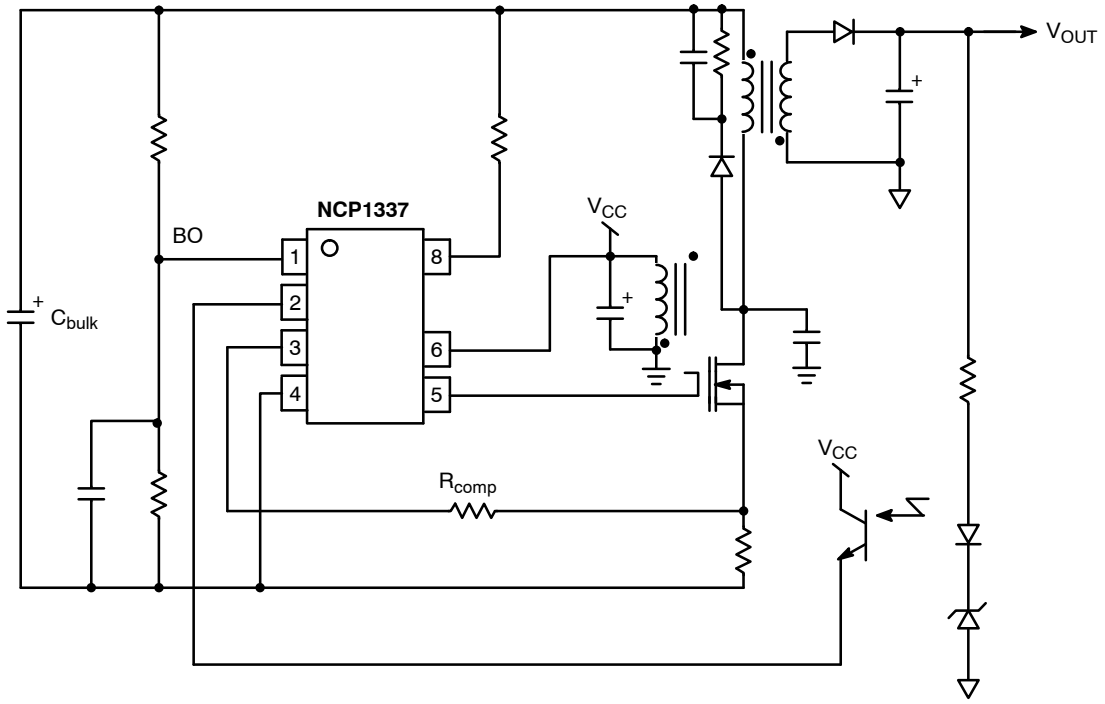

Figure 1. NCP1337 Typical Application Example

PIN BY PIN IMPLEMENTATION

Pin 1: "BO" pin
Brown−out

SMPS are designed for a given input voltage range. When the input voltage is too low, the power supply tends to compensate by sinking more current from the line to deliver the same output power. As a result, the power components may suffer from an excessive heating and ultimately the SMPS may be destroyed. Another consequence is that as when the electricity network weakens, its voltage tends to decrease, and as in this case SMPS tend to sink more current, electricity network gets weaker and weaker and eventually collapses (it is the reason why this protection is called 'brown−out' protection).

A simple solution to protect at the same time the power supply and the network is to stop the SMPS controller when the input voltage is too low. For this purpose Pin 1 offers a comparator with hysteresis able to stop the controller if the voltage applied is too low. By applying an image of the input voltage on the pin, it becomes possible to authorize operation above a certain level of mains only. The controller monitors this voltage and when the Pin 1 voltage is too low (i.e., when Vpin1 is below 500 mV), the controller stops pulsing and keeps disabled until this level exceeds 500 mV. In order to prevent the instabilities that could result from the input voltage ripple, an hysteresis is programmable thanks to an internal 10 μA current source which is turned on when the voltage on BO pin is above 500 mV. The brown−out protection is not latched: when the input voltage (V_{IN}) is below the target, the controller stops pulsing but it recovers operation, after a soft−start, as soon as V_{IN} goes back within the acceptable range.

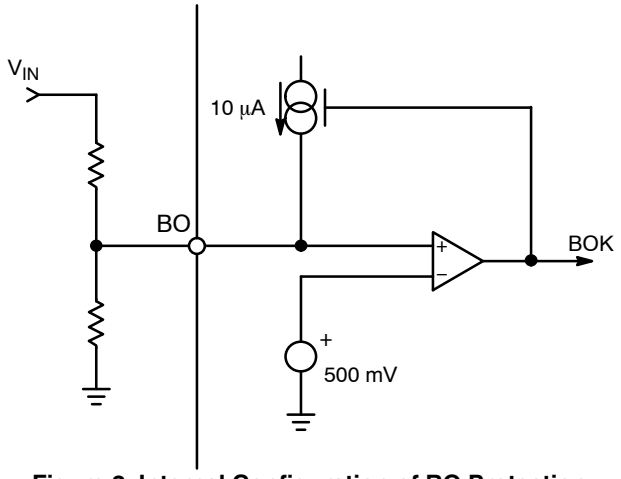

Figure 2. Internal Configuration of BO Protection

Startup level is directly given by the resistor divider connected between V_{IN} and BO pin, knowing that the threshold of the internal comparator is 500 mV.

Once the controller has started, an internal 10 μA current source is activated and flows out of BO pin, creating a voltage offset across the equivalent resistance of the resistor divider.

Those two conditions lead to the following equations:

$$\frac{R_{BOhigh} + R_{BOlow}}{R_{BOlow}} \cdot V_{IN(ON)} = 500\ mV \quad \text{(eq. 1)}$$

and

$$\frac{R_{BOhigh} + R_{BOlow}}{R_{BOlow}} \cdot V_{IN(OFF)} + \frac{R_{BOhigh} \cdot R_{BOlow}}{R_{BOhigh} + R_{BOlow}} \cdot 10\ \mu A = 500\ mV \quad \text{(eq. 2)}$$

With $V_{IN(ON)}$ the turn−on and $V_{IN(OFF)}$ the turn−off input voltages.

Solving these equations gives the recommended values for R_{BOhigh} and R_{BOlow}, but in reality there could be a non−negligible ripple on the DC input voltage (depending on the size of the bulk capacitor), and it may be necessary to increase the hysteresis in order to obtain the desired turn−off level.

It is as well recommended to add a capacitor between BO pin and ground to filter any noise, and to ensure a DC voltage. But this capacitor value should be small enough otherwise it may introduce a delay between input voltage collapsing and power supply turn−off (a 10 nF capacitor gives good results).

We will see later that Overpower Protection is dependent on V_{BO} voltage: to have an accurate protection, V_{BO} should be proportional to the input voltage of the SMPS stage. But in the case there is a front−end PFC stage, there is a dilemma: once PFC has started, V_{BULK} is not any more an image of the mains voltage: it means that even if V_{IN} goes below $V_{IN(OFF)}$, PFC stage will still try to maintain V_{BULK} high, and the Brown−out protection is not effective. So connecting BO to the real V_{IN} is recommended, even if overpower protection is less accurate. A solution to improve this protection is to use a “follower boost” type of PFC in which the output follows the input.

Latch

This pin also performs a second function: it provides two comparators to temporarily (autorecovery) or permanently (latched) stop the controller by an external condition (Figure 3).

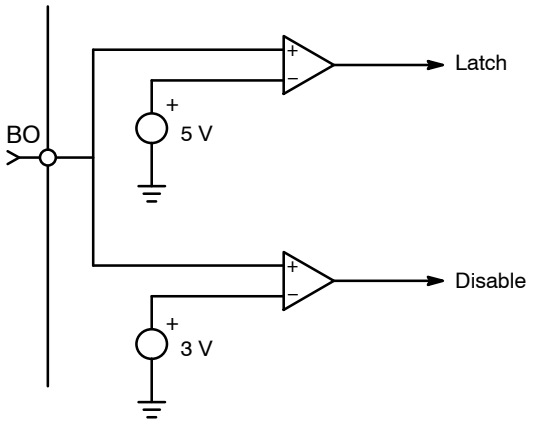

Figure 3. Internal Implementation of Disable and Latch Comparators

To perform a disable function, the voltage on BO pin must go above 3 V, and over 5 V for a latch function.

In case of a primary OVP, where V_{AUX} or V_{CC} is monitored, a direct connection of a zener diode between the monitored voltage and BO pin is not able to toggle the Latch comparator: in such configuration, only the disable function will be activated.

To have a latched protection, the OVP signal must be buffered with a high gain PNP transistor (see Figure 4) in order to raise BO voltage above 5 V faster than the SMPS reaction to the disable comparator (which is toggled first).

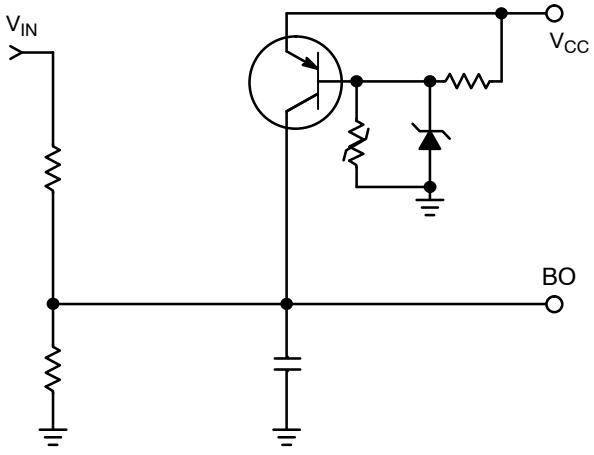

Figure 4. How to Perform a Latched OTP or OVP

Pin 2: “FB” pin

In order to simplify the implementation of a primary regulation, the FB circuitry is a shunt regulator with a fixed voltage of 3 V, combined with a current to voltage translator. This means that the FB information is a current, which is internally converted to a voltage that sets the setpoint for the current−mode control. In case of a secondary regulation, the optocoupler transistor must be connected between V_{CC} and FB pin.

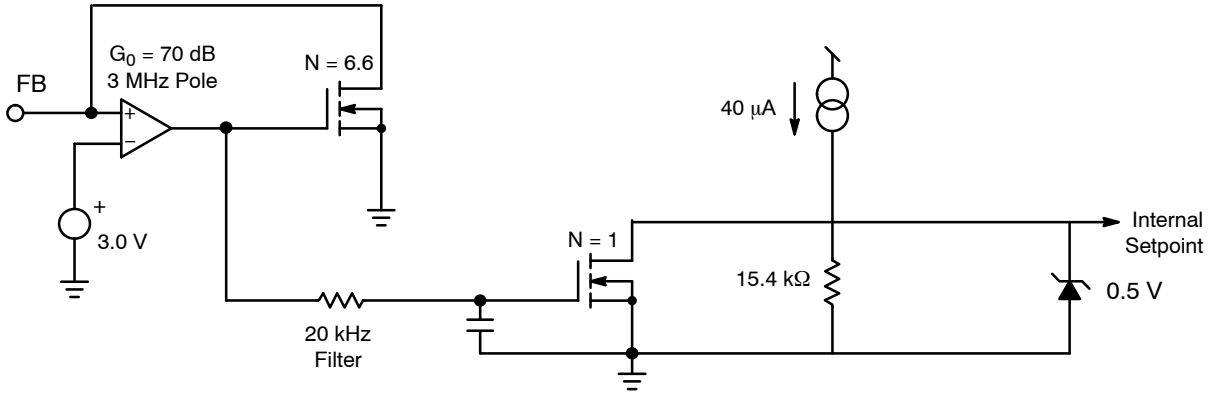

Figure 5. Internal Circuitry of FB Pin

Maximum CS pin voltage $V_{CSlimit}$ is 0.5 V, corresponding to a FB current of 50 μA: when the current on FB pin is lower than 40 μA, an internal flag $I_P$flag is raised and the fault timer is started. If $I_P$flag stays asserted until TIMER pin voltage reaches 5 V, FAULT is detected and the controller enters protection mode: pulses are stopped, and V_{CC} capacitor is discharged by the internal current consumption ICC3 down to VCC_{LATCH}. Then the V_{CC} capacitor is charged again to VCC_{ON} and discharged to VCC_{LATCH} without attempting to restart. A new startup phase takes place only the second time V_{CC} reaches VCC_{ON} after the fault detection. This ensures a low−frequency burst mode safe for the power supply if the overload is still present. When the faulty condition disappears, the controller resumes normal operation after the next restart attempt (Figure 6).

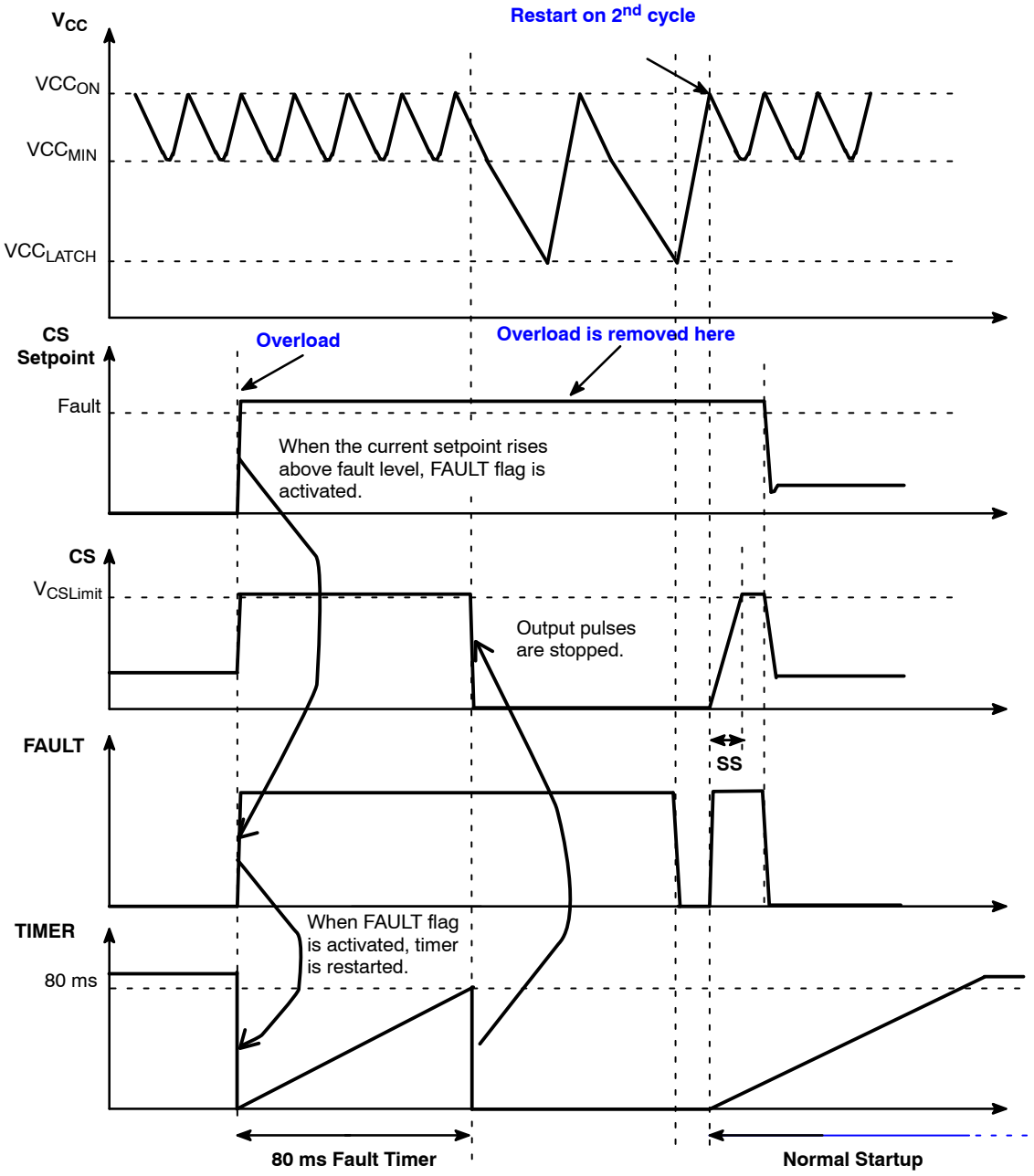

Figure 6. Typical Behavior in Overload Conditions

Pin 3: "CS" Pin

This pin performs two distinct functions: primary peak current reading and compensation for overpower protection.

Peak Current Reading

It is classically performed through the reading of the voltage appearing through a sense resistor connected between switching MOSFET's source and ground. The internal maximum current sense level $V_{CSlimit}$ is 0.5 V, so R_{SENSE} must be calculated by Equation 3, with I_{pkMAX} the maximum peak primary current at the lowest input voltage and maximum output load.

$$R_{SENSE} = \frac{0.5}{I_{pkMAX}} \quad \text{(eq. 3)}$$

A leading edge blanking (LEB) prevents any spike appearing during the first 350 ns after T_{ON} to toggle falsely the internal current sense comparator. This LEB is usually enough, but if for some reasons an additional filtering is necessary, it is still possible to add externally an RC filter.

Overpower Compensation

In the quasi−resonant mode of operation, the slope of the current during ON time is;

$$\frac{V_{IN}}{L_P} \quad \text{(eq. 4)}$$

and during OFF time, it is;

$$\frac{N \cdot V_{OUT}}{L_P} \quad \text{(eq. 5)}$$

Thus for a given peak current I_{pk}, T_{ON} is shorter at high V_{IN} than at low V_{IN}, and T_{OFF} is constant: so the switching frequency F_{SW} is higher at high V_{IN} (see Figure 7).

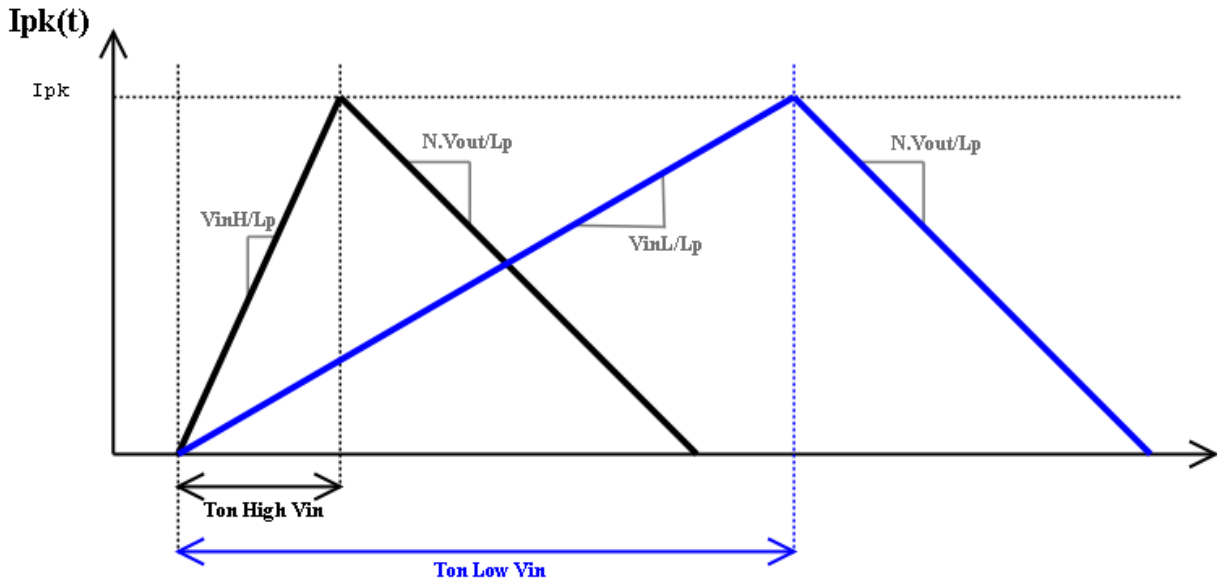

Figure 7. T_{ON} Behavior at a Biven I_{pk} for Different V_{IN}

Knowing Equation 6 (with η the efficiency), it is clear that for a given I_{pk}, P_{OUT} is higher at high V_{IN} than at low V_{IN}. So for a constant output power, the peak current is lower at high V_{IN} than at low V_{IN} (see Figure 8).

$$P_{OUT} = \eta \cdot P_{IN} = \eta \frac{1}{2} \cdot L_P \cdot I_{pk}^2 \cdot F_{SW} \quad \text{(eq. 6)}$$

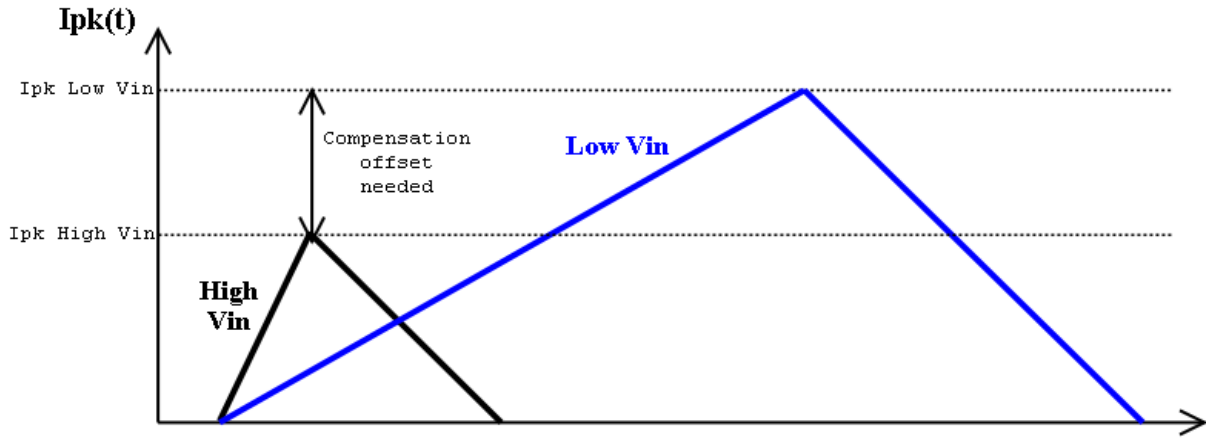

Figure 8. I_{pk} Behavior at a Given P_{OUT} for Different V_{IN}

As the overload detection of NCP1337 is based on peak current detection, if an overpower protection is needed the voltage applied on CS pin at P_{OUTmax} must be the same at high V_{IN} and low V_{IN}. The solution consists in adding a compensation offset proportional to V_{IN} to the voltage sensed across the sense resistor. NCP1337 offers the possibility to easily create this offset by activating an internal current source proportional to V_{BO} during T_{ON}: this current flows out of pin CS and create an offset proportional to V_{BO} (which is proportional to V_{IN}) through a series resistor (see Figure 9).

To further simplify the design of the compensation, the offset current is null when V_{BO} is equal to 0.5 V, corresponding to the minimum allowed input voltage.

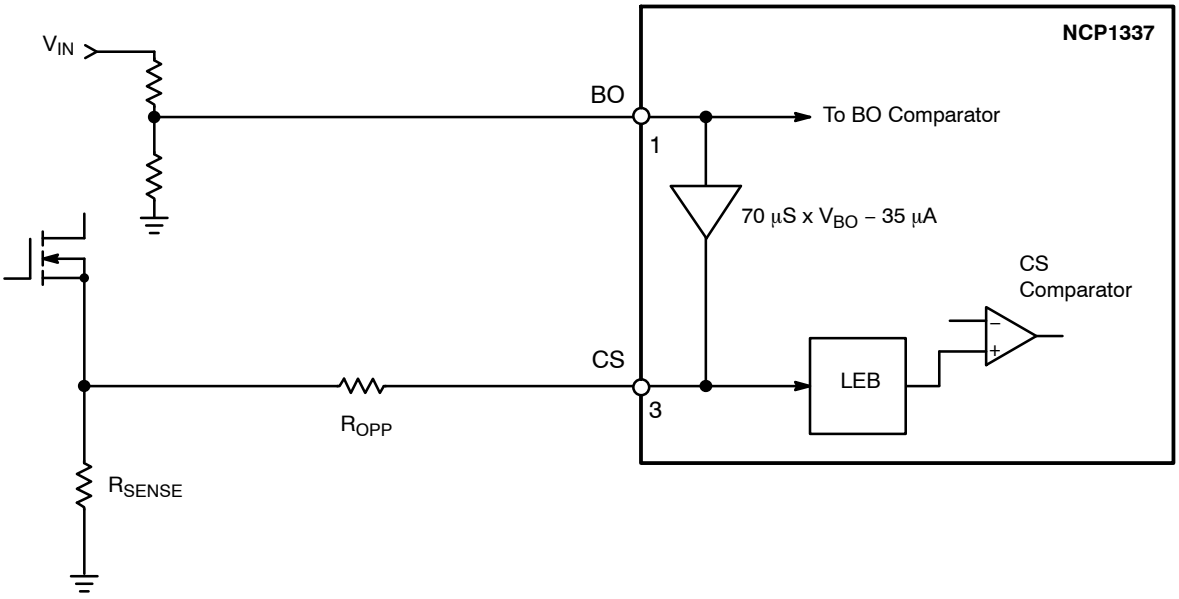

Figure 9. Internal Overpower Compensation Circuitry on CS Pin

Design Steps:

- Estimate peak current I_{pk} values at minimum V_{IN} and maximum V_{IN} for the maximum output power allowed. By neglecting the delay between core reset and the real valley (it is small compared to the switching period at high output power), we can estimate I_{pk} at a given V_{IN} by Equation 7. Thus calculate $I_{pkmaxLV}$ and $I_{pkmaxHV}$, respectively max peak currents at low and high input voltages.

$$I_{pk} = \frac{2 \cdot P_{OUT}}{\eta} \cdot \left(\frac{1}{V_{IN}} + \frac{1}{N \cdot V_{OUT}} \right) \quad \text{(eq. 7)}$$

- Calculate the sense resistor to allow the maximum peak current to flow at the minimum input voltage:

$$R_{SENSE} = \frac{0.5}{I_{pkMAX\ LV}} \quad \text{(eq. 8)}$$

- As we know what is the value of V_{BO} for a given V_{IN}, we can calculate the needed offset resistor R_{OPP} knowing that:

$$V_{OFFset} = R_{OPP} \cdot (V_{BO_{HV}} \cdot 70 \cdot 10^{-6} - 35 \cdot 10^{-6}) \quad \text{(eq. 9)}$$

Which gives the following equation.

$$R_{OPP} = \frac{I_{pkMAX\ LV} - I_{pkMAX\ HV}}{I_{pkMAX\ LV}} \cdot \frac{0.5}{V_{BO_{HV}} \cdot 70 \cdot 10^{-6} - 35 \cdot 10^{-6}} \quad \text{(eq. 10)}$$

Pin 4: "GND" Pin

Reference ground for the controller.

Pin 5: "DRV" Pin

This pin performs two distinct functions: it drives the switching MOSFET and detects the "valley" of the drain voltage thanks to the "Soxyless" detector.

MOSFET Driving

By offering up to ±500 mA peak, this pin allows to drive large Q_G MOSFETs without adding any additional components.

Valley Detection

The “Valley point detection” is based on the observation of the Power MOSFET Drain voltage variations. When the transformer is fully demagnetized, the Drain voltage evolution from the plateau level down to the V_{IN} asymptote is governed by the resonating energy transfer between the L_P transformer inductor and the global capacitance present on the Drain. These voltage oscillations create a current oscillation in the parasitic capacitor across the switching Mosfet (modelized by the C_{RSS} capacitance between Gate and Drain): a negative current (flowing out of DRV pin) takes place during the decreasing part of the Drain oscillation, and a positive current (entering into the DRV pin) during the increasing part (see figure 10).

The Drain valley corresponds to the inversion of the current (i.e. the zero crossing): by detecting this point, the NCP1337 can switch on when the drain voltage is minimum, and thus always ensure a true valley turn−on.

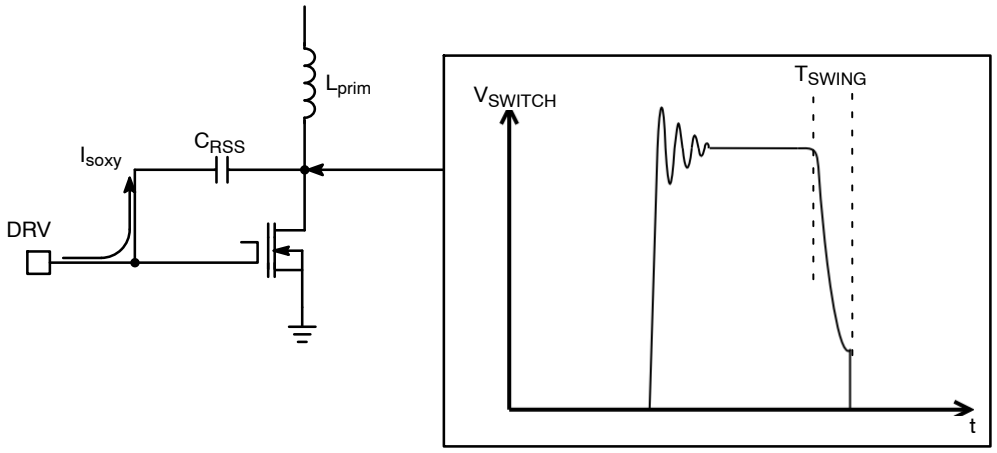

Figure 10. Soxyless Concept

The current in the Power MOSFET gate is:
$I_{GATE} = V_{RINGING} / Z_C$ (with Z_C the capacitance impedance), so $I_{GATE} = V_{RINGING} \bullet (2 \bullet \pi \bullet F_{RES} \bullet C_{RSS})$

The magnitude of this gate current depends on the MOSFET, the resonating frequency F_{RES} and the voltage swing $V_{RINGING}$ present on the Drain at the end of the plateau voltage.

The dead time T_{SWING} is given by the equation:

$$T_{SWING} = 0.5/F_{RES} = \pi * \sqrt{L_P * C_{DRAIN}} \quad \text{(eq. 11)}$$

Where L_P is the primary transformer inductance and C_{DRAIN} the total capacitance present on the MOSFET Drain.

This capacitance includes the snubber capacitor if any, the transformer windings stray capacitance plus the parasitic MOSFET capacitances C_{OSS} and C_{RSS}.

The detector’s threshold has been designed to work perfectly with the most recent high voltage MOSFETs for which the C_{RSS} capacitance is usually in the range of 12 pF to 15 pF. But it will work perfectly in most situations even with a C_{RSS} as low as 5 pF or as high as 50 pF.

However two cases can occur that will require an additional tuning:

- The detector is not sensitive enough (C_{RSS} is too small): the first valley(s) is (are) detected, but not the following ones, leading to an instability at light load (see Figure 11). In this case it is necessary to increase the gate to drain capacitance by adding an external capacitor (see Figure 12). A 4.7 pF or 10 pF capacitor is enough to increase the sensitivity of the detector and cancel the instability. This added capacitor must be a high voltage model as it must sustain the drain voltage.

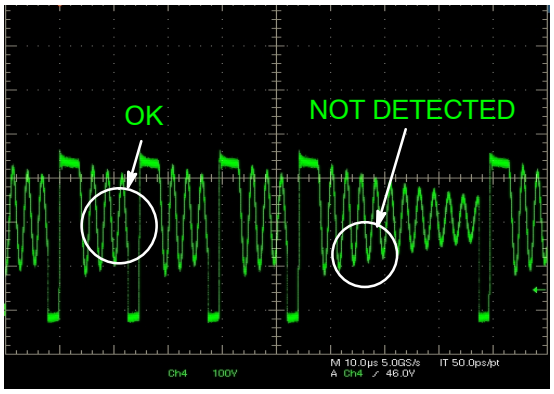

Figure 11. Instability at Lower Load

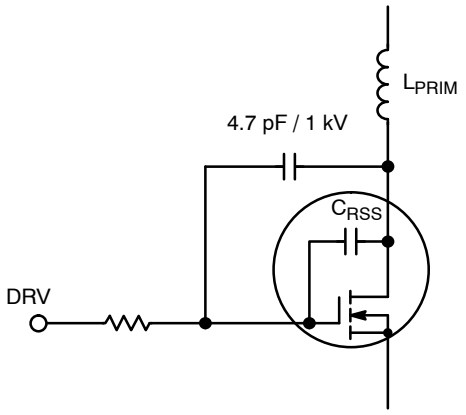

Figure 12. External Gate−to−Drain Capacitor

- The detector is too sensitive (C_{RSS} is too big): in multiple−output applications the small oscillation created by the early demagnetization of one of the output windings is detected, leading to a CCM operation (see Figure 13). A 470 pF or 1 nF capacitor connected between MOSFET's gate and ground reduces the sensitivity (see Figure 14).

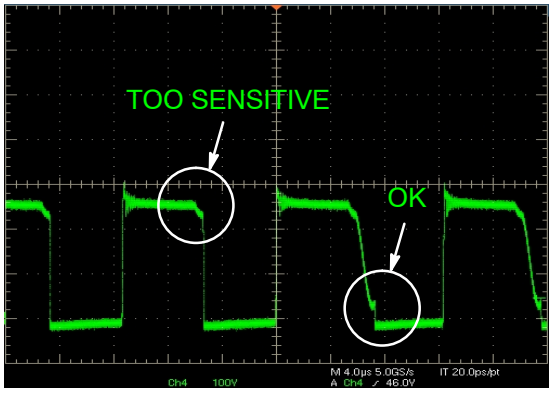

Figure 13. Instability with Multiple Outputs

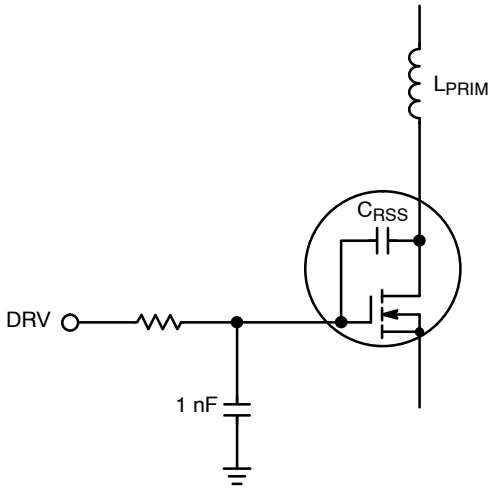

Figure 14. Gate−to−Ground Capacitor

Finally, if the NCP1337 is not connected directly to the MOSFET, but through an external driver or a buffer, an external gate−to−drain capacitor must be added as there is no current path from the drain node to the DRV Pin (Figure 15).

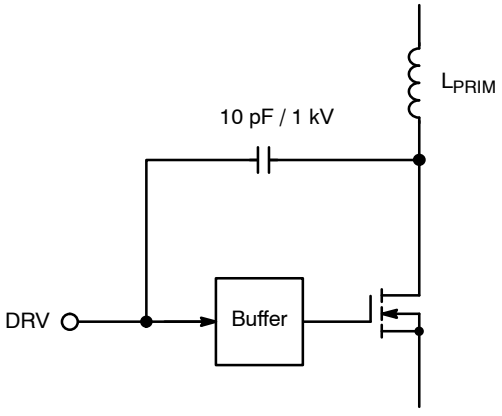

Figure 15. External Gate−to−Drain Capacitor When a Buffer is Used

Pin 6: "V_{CC}" Pin

This is the supply pin for the controller. NCP1337 features a high voltage current source between Pins 8 ("HV") and 6 ("V_{CC}") which turns on during startup to charge the V_{CC} capacitor, but also operates in Dynamic Self−Supply mode (DSS), alternatively turning on and off to maintain the voltage on V_{CC} pin between VCC_{ON} and VCC_{MIN}. If the current consumption on the DRV pin is too high for the DSS capability, or for the power dissipated in the package, an auxiliary supply should take the hand and supply the V_{CC} once the controller has started. Using an auxiliary supply also helps to reduce the standby power in no−load conditions, by supplying the NCP1337 from a low voltage instead of the high input voltage.

The V_{CC} capacitor is selected by taking into account the startup time, the duty ratio in protection mode and the ability to maintain V_{CC} above V_{CCmin} in order to disable the startup circuit at light loads.

- The startup time (see Figure 16)

The startup time $T_{STARTUP}$ is the sum of T1 and T2, which both depend on the V_{CC} capacitor:

$$T_{STARTUPMAX} = C_{VCC} \cdot \frac{VCC_{INHIB}}{IC2_{MIN}} + \frac{VCC_{onMAX} - VCC_{INHIB}}{IC1_{MIN}} \quad \text{(eq. 12)}$$

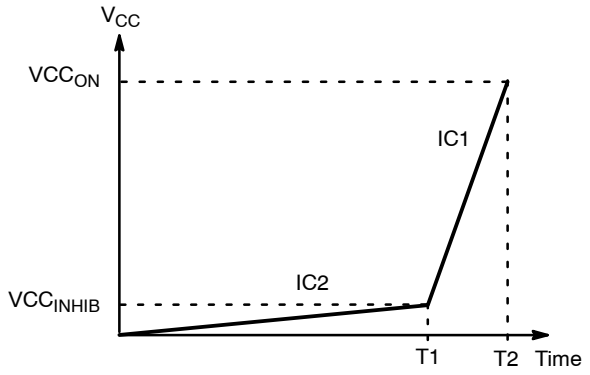

Figure 16. Dual Startup Current Source

- The duty ratio of the protection mode: the working period duration is given by the internal Fault timer, but the "OFF" period is dependent on the V_{CC} capacitor charging and discharging times (see Figure 17).

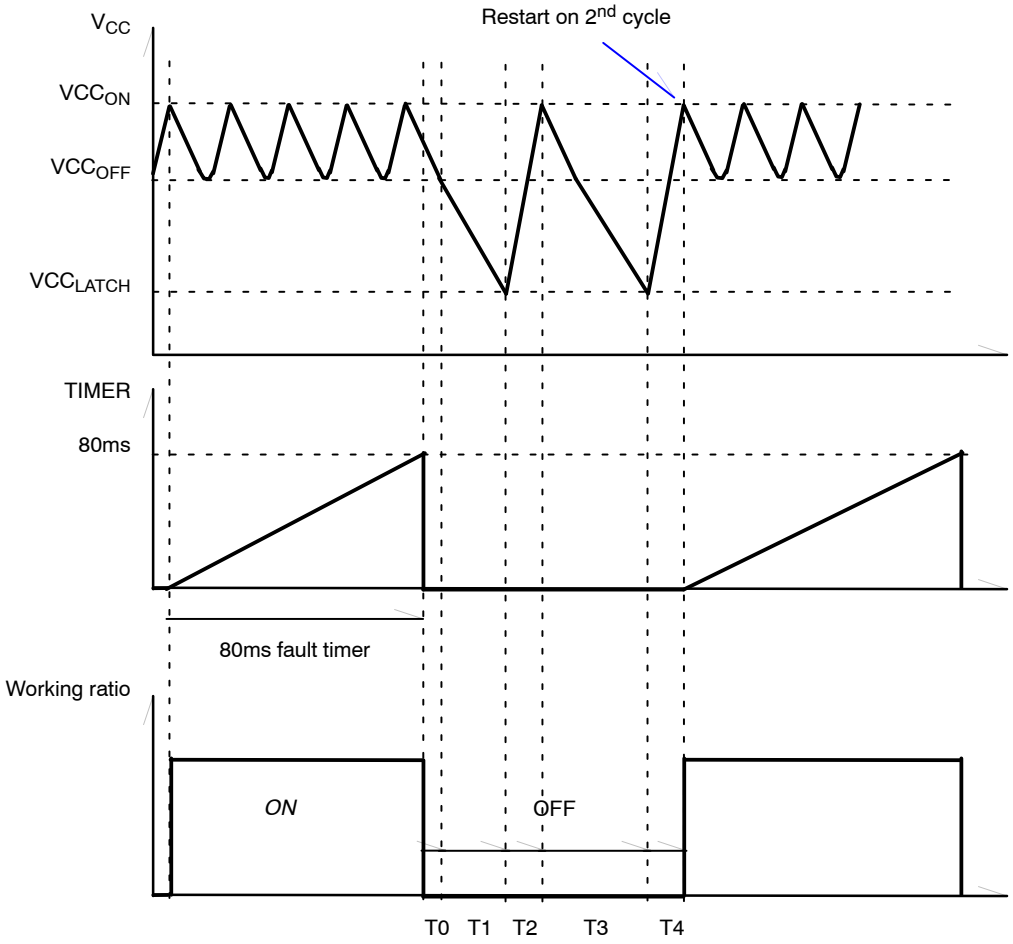

Figure 17. Duty Ratio in Short−Circuit Conditions

The off time duration of the short−circuit protection mode T_{SCoff} is the sum of two discharging and two charging times of the V_{CC} capacitor. By neglecting T0, we can estimate a minimum value for T_{SCoff}:

$$T_{SCoffmin} = C_{VCC} \cdot \left(2 \cdot \frac{VCC_{MINmin} - VCC_{LATCHmax}}{I_{CC3}} + 2 \cdot \frac{VCC_{ONmin} - VCC_{LATCHmax}}{I_{C1\,min}} + \frac{VCC_{ON} - VCC_{MIN}}{I_{CC3}}\right) \quad \text{(eq. 13)}$$

- The amount of energy stored and thus the ability to keep V_{CC} above VCC_{MIN} (and thus not activate the DSS) when the power supply operates in low load conditions. If a big capacitor is needed to run in auxiliary supply mode at no load, but the startup time is too long, a solution consists in splitting the V_{CC} capacitor into two different components: a tank capacitor is used to store energy for no−load operation, whereas the V_{CC} capacitor stays small enough to ensure a fast startup (Figure 18).

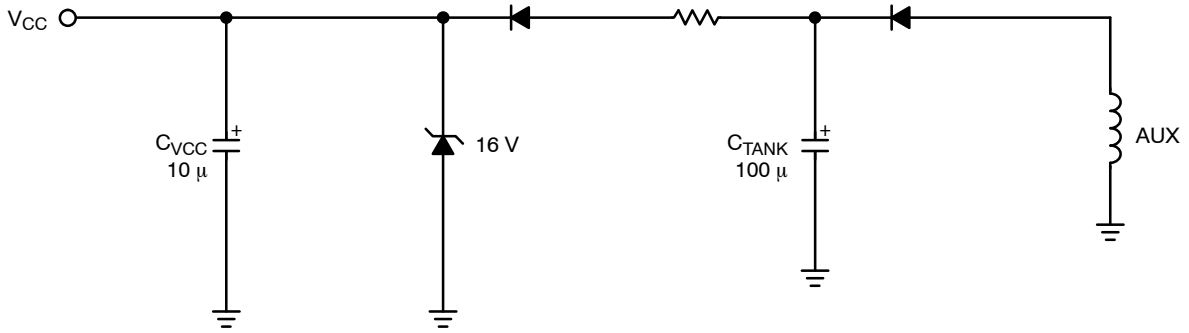

Figure 18. Split Capacitor on V_{CC} Pin

Pin 7: Unused Pin

This pin is left unconnected to ensure a wider creepage distance between the high voltage pin and the V_{CC} pin.

Pin 8: "HV" pin

An internal current source is connected between the HV and V_{CC} pins, and is able to supply the controller from a minimum dc voltage of 60 V. It is highly recommended to add a series resistor R_{HV} between the high voltage rail and the pin to protect NCP1337 against negative spikes that could appear due to a resonance between the primary inductor and the bulk capacitor.

Power Dissipation

When the NCP1337 is directly supplied from the dc rail through the internal DSS circuitry, the DSS being an auto−adaptive circuit (e.g. the ON/OFF Duty Cycle adjusts itself depending on the current demand), the current flowing through the DSS is the direct image of the NCP1337 current consumption. As a result, the total power dissipation can be estimated using:

$$\left(V_{HVdc} - \frac{VCC_{ON} - VCC_{MIN}}{2}\right) \cdot I_{CC2} \quad \text{(eq. 14)}$$

The real current consumption is actually given by the sum of the internal consumption of the NCP1337 and the driving current I_{DRV} for the selected MOSFET. The best method to evaluate this total consumption is probably to run the final circuit from a 50 Vdc source applied to HV pin and measure the average current flowing into this pin. Replacing ICC2 by this measured current will give a more accurate estimation of the dissipated power.

Eventually the drive current can also be calculated by:

$$I_{DRV} = F_{SW} \cdot Q_G \quad \text{(eq. 15)}$$

With F_{SW} the switching frequency and Q_G the selected MOSFET's gate charge.

The maximum allowable power dissipation P_{MAX} can be computed knowing the maximum operating ambient temperature, T_{Amax}, together with the maximum allowable junction temperature T_{Jmax}:

$$P_{MAX} = (T_{Jmax} - T_{Amax}) \cdot R_{\theta JA} \quad \text{(eq. 16)}$$

with $R_{\theta JA}$ the junction−to−air thermal resistance, which notably depends on the package.

In case the power dissipation exceeds P_{MAX}, several solutions exist to rectify the problem:

- The first one consists in adding some copper area around the NCP1337 package footprint, which will help to decrease the junction−to−air thermal resistance.
- Calculate the resistor R_{HV} in series with the HV pin in order to split the power budget between this resistor and the package. The resistor is calculated by leaving at least 60 Vdc on Pin 8 at minimum input voltage (you can refer to the application note AND8069 available from www.onsemi.com).
- If the power consumption budget is really too high for the DSS alone, connect a diode between the auxiliary winding and the V_{CC} pin, which will disable the DSS operation (by ensuring $V_{CC} > VCC_{MIN}$).

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